Andrew Adiletta

ajadiletta@wpi.edu

Contact

244 Sawyer Road
Bolton, Mass 01740
978-735-9666

Education

Worcester **P**olytechnic **I**nstitute
Worcester, MA
BS ECE (2019-2022) 4.0/4.0
MS ECE (2022-2023) 4.0/4.0
MS focus: Hardware Security

Scholarships

Dearborn Foundation-Engineering Scholarship

WPI Presidential Scholarship

Key Skills

Languages: Java, Javascript, C#, C/C++, PHP, SQL, Python, Batch, HTML, CSS, Swift, Racket, Matlab, Verilog

Tools: GNU GDB, Xilinx Vivado, Blender, Solidworks

Related Courses: Calculus 4; ECE 2010; Differential Equations; Physics Mechanical / E&M; Accelerated Program Design, ECE Sensor & Circuits; Digital Circuit Design; Linear Algebra; Probability; Computer Architecture, Modern Physics, Statistics, Advanced FPGA Design , Electromagnetism, Power Control Systems, Operating Systems, Real Time Operating Systems, Discrete Signals, Advanced Cryptography

Objective

Seeking challenging opportunities in electrical and computer engineering with a focus on hardware security, where I can apply my skills in research, software development, and innovation.

Experience

2022 to 2023 (12 months): WPI – Vernam Labs - Graduate Level Research: Fault Injection Attacks on Stack and Registers: Primary author for a paper currently under peer-review, focused on a groundbreaking technique for attacking secure stack and register variables. Novel approach leverages Rowhammer to inject faults in stack and register variables, effectively bypassing stack Address Space Layout Randomization (ASLR) in the Linux kernel, and compromising authentication in critical software such as SUDO, OpenSSH, MySQL, and OpenSSL. Research also presents countermeasures against crypto vulnerabilities. To overcome significant challenges associated with this technique, I introduced innovative methods for mapping stack variables to flippy pages, addressing stack ASLR with random page offsets, ensuring flip reproducibility, and maintaining synchronization.

2021 to 2022 (6 months): WPI – Vernam Labs - Graduate Level Research: Fault Injection Attacks on ML: Working at the WPI cryptography and cybersecurity research facility, Vernam Labs (http://vernam.wpi.edu/), studied fault injection attacks on DRAM and wrote bachelor's thesis on the subject. Developed mechanisms for targeted fault injections on protected areas in memory which can be used for privilege escalation. Coauthored a research paper submitted to CCS on backdoor injection attacks on machine learning algorithms using fault injection, to modern DDR4 memory.

2021 (3 months): **Postal Museum of London Consultation: Team Management and Digital Asset Management,** Consulted with the Postal Museum of London to recommend an optimal software configuration for their Digital Asset Management (DAM) and Digital Preservation Systems (DPS). Utilizing a six-step approach, identified Third Light Chorus and Preservica as the preferred DAM and DPS solutions, respectively. Both cloud-based systems offered user-friendly interfaces, advanced permissions features for standardized metadata entry, and improved organization. I also advised the museum to implement more stringent metadata entry processes, train staff, and collaborate with a research team to ensure successful system integration.

Intel Co-op 2021 (8 months): **Fault Tolerant Validation Utility,** Continuing work from previous Co-op expanding on graph-based validation checker, as well as reducing runtime on checker and improving resource efficiency. Additionally, produced internal white paper on the benefits of graph-based validation, leading to widespread adoption of the technology in the company. Implemented validation using the structure on various power systems related flows for SoC servers. This included sophisticated systems to monitor voltage frequency curves for SoC power management.

Intel Co-op 2020 (8 months) - Fault Tolerant Validation Utility, Part of power management validation at Intel, tasked to design a system in python that can validate power flows on pre-silicon architectures. The project consisted of building a framework of recursive checking structures that could intelligently determine problems outlined by a pattern of checks defined by a user, and report issues in a readable format. Additionally, defining checks for multiple power flows to use as models for other employees as well as used in active checking for the future architectures. The product was a convenient API that could be used on validation output samples many thousand lines long to determine potential issues with power flows and sequences in an efficient fashion, as well as organizing PM checks into readable sub-structures that improved productivity of PM validation at Intel. At end of co-op, presented product to Intel Validation for their future use.

Intel Internship Summer 2019 – Binomial Options Pricing, Developed an original implementation for binomial option pricing for a Xeon processor, and compared result to real time options data, proving validity of implementation. Then developed an algorithm for use on a new Intel parallel processor architecture that computes the future value of a trading option using binomial option pricing techniques while not using recursion. The method implemented a novel triangular memory consumption model to produce a binomial tree due to lack of development in recursive function in this early stage architecture tools compiler. Learned and wrote test implementation in python/bash for use with netbatch on Intel's High Performance Computers, and wrote algorithm in C. Required debug of parallel processor assembly code. Goal of project was to prove performance of new Intel data parallel processor. At end of Internship, presented project at VSSAD forum which is architecture advanced development group.

2019 - WPI Physics Teaching Assistant, Based on abilities and good standing in the Physics department, I was asked by the head of the department to be a teaching assistant for Physics 1110 and 1111 for mechanics/E&M respectively. This is a position unusual for an incoming Freshman, but I was asked based on my abilities to explain concepts and work collaboratively, and I provided office hours, tutoring, and grading papers for ~80 students.

2018-2019 – Traveling Salesman Problem (TSP), developed an engineering project for the Mass Science and Engineering Fair, based on applying an original Genetic Algorithm to the Traveling Salesman Problem and examining performance against a generic genetic algorithm. Presented results in early 2019 at WPI then at MIT in May. Also, in order to learn the Apple Swift development environment, developed a TSP game which is available on the Apple App store: https://itunes.apple.com/us/app/dot-route/id1456620758?ls=1&mt=8

Activities

WPI Kryptos Codebreaking Team;
Ham Radio Club (earned Technician's License);
Collab Lab; WPI Running Club; WPI Underwater Hockey

Eagle Scout, RA position, WA Senior Science and Engineering Award; WA Geometry Award, Pianist/Euphoniumist/Guitar Player, High School Captain of 3 teams.

References

[Available upon request.]